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(54) SOLID-STATE IMAGE PICKUP DEVICE AND ITS DRIVE METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To eliminate remaining fixed pattern noise of longitudinal stripes resulting from dispersion in the characteristic of circuits as well as fixed pattern noise resulting from dispersion in characteristics of picture elements.
SOLUTION: In an amplifier type solid-state image pickup device that provides an output of a voltage for a signal from a pixel 11, each input of a load capacitor 16 and a dummy capacitor 17 is connected to an output terminal of a sampling switch 15, and each output of the capacitors 16, 17 is connected properly to a reference potential line 18 via reference switches 19, 20. Furthermore, an output of the load capacitor 16 is connected to an input terminal of a vertical output circuit 21 and a signal voltage Vsigl in a bright state and a signal voltage Vsigd in a dark state are read through the same signal path to eliminate not only a fixed pattern noise resulting from dispersion in the characteristic of the pixel 11 but also a fixed pattern noise of longitudinal stripes resulting from dispersion in the characteristic of the circuit.

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CLAIMS

[Claim(s)]

[Claim 1] Two or more pixels arranged in the shape of a matrix, and the 1st switching means by which the end was connected to the perpendicular signal line to which each outgoing end of two or more of said pixels was connected per train, The 1st and the 2nd are recording means which one edge each was connected to the other end of said 1st switching means in common, The solid state camera characterized by having a perpendicular output circuit containing the level selecting switch connected between the other end of the 2nd and 3rd switching means connected, respectively between each other end of the said 1st and 2nd are recording means, and a reference potential point, and said 1st are recording means, and a level signal line for every train.

[Claim 2] Said perpendicular output circuit is a solid state camera according to claim 1 characterized by consisting of a level selecting switch connected between the source follower circuit where the input edge was connected to the other end of said 1st are recording means, and the outgoing end of said source follower circuit and said level signal line.

[Claim 3] The solid state camera according to claim 1 characterized by having the circuit which takes the difference of two signals read to said level signal line in order through said perpendicular output circuit.

[Claim 4] Two or more pixels arranged in the shape of a matrix, and the 1st switching means by which the end was connected to the perpendicular signal line to which each outgoing end of two or more of said pixels was connected per train, The 1st and the 2nd are recording means which one edge each was connected to the other end of said 1st switching means in common, The 2nd and 3rd switching means connected, respectively between each other end of the said 1st and 2nd are recording means, and a reference potential point, Are the drive approach of the solid state camera equipped with the perpendicular output circuit containing the level selecting switch connected between the other end of said 1st are recording means, and a level signal line for every train, and it sets at a level blanking period. First, make said 1st switching means turn on by the ON state of said 2nd switching means, and the signal at the time of ** is sampled. Then, make said 1st switching means turn off and the signal at the time of said ** is held for said 1st accumulation-of-electricity means. Next, said 3rd switching means which is made to turn off said 2nd switching means and is in an OFF state continuously is made to turn on. Next, make said 1st switching means turn on again, sample the signal at the time of dark, and make said 1st switching means turn off again, and hold the signal at the time of said dark for said 2nd accumulation-of-electricity means, and, subsequently to a level shelf-life, it is set. The drive approach of the solid state camera characterized

by reading the electrical potential difference of the output side of said 1st accumulation-of-electricity means to said level signal line, making said level selecting switch turn on, making said 2nd switching means turn on continuously, and reading a reference potential to said level signal line.

[Claim 5] The drive approach of the solid state camera according to claim 4 characterized by taking the difference of the electrical potential difference of the output side of the 1st [said] accumulation-of-electricity means transmitted almost simultaneously on a time-axis with said level signal line, and said reference potential.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the magnification mold solid state camera which the pixel itself has a magnification function and outputs the signal of a pixel on an electrical potential difference, and its drive approach about a solid state camera and its drive approach.

[0002]

[Description of the Prior Art] as a magnification mold solid state camera -- CMD (Charge Modulation Device), BASIS (Base Stored Image Senser), and BCMD (Bulk Charge Modulation Device) etc. -- it is known. Since active elements, such as metal-oxide-semiconductor structure, are used and the pixel is constituted from this

magnification mold solid state camera in order to give a magnification function to the pixel itself, the variation in the properties (threshold electrical potential difference Vth etc.) of an active element will ride on a picture signal as it is. Since the variation in this property has the value of immobilization in each pixel, it appears as a fixed pattern noise (FPN;Fixed Patern Noise) on a screen.

[0003] The conventional example of the magnification mold solid state camera made that the fixed pattern noise resulting from the property variation of this pixel should be removed is shown in drawing 7 . In this drawing, many pixels 101 are arranged in the shape of a matrix, the control-input edge of each pixel 101 is connected to each of the perpendicular selection line 102 per line, and each outgoing end is connected to each of the perpendicular signal line 103 per train. One edge each of the perpendicular selection line 102 is connected to the outgoing end of each line of the vertical-scanning circuit 104. The vertical-scanning circuit 104 is constituted by the shift register etc., and outputs vertical-scanning pulse phiV (--, phiVm, phiVm+1, --) in order.

[0004] Each drain of two sampling switches 105s and 105n which consist of NchMOS transistors is connected to each of the perpendicular signal line 103. Of operation pulse phiOPS for sampling the signal level at the time of ** before the pixel reset outputted from a pixel 101 is impressed to the sampling switch 105s gate. Moreover, of operation pulse phiOPN for sampling the signal level at the time of the dark after the pixel reset outputted from a pixel 101 is impressed to the sampling switch 105n gate.

[0005] Each sampling switches [105s and 105n] source is connected to one edge each of two capacitors 106s and 106n, respectively. It is prepared in order that these capacitors 106s and 106n may hold the signal level at the time of **, and the signal level at the time of dark, respectively, and each other end of both is grounded. Each sampling switches [105s and 105n] source is further connected to each drain of two level selecting switches 107s and 107n which consist of NchMOS transistors, respectively.

[0006] Each level selecting switches [107s and 107n] source is connected to the level signal line 108, and each gate is connected to the outgoing end of each train of the horizontal scanning circuit 109. The horizontal scanning circuit 109 is constituted by the shift register etc., and outputs horizontal scanning pulse phiH (--, phiHn, phiHn+1, --) for making 107s of level selecting switches, and 107n of level selecting switches turn on in order for every train. The level signal line 108 is connected to the input edge of the water Hiraide force circuit 110. The outgoing end of the water Hiraide force circuit 110 is connected to the input edge of the CDS (correlation duplex sampling) circuit 111.

[0007] Next, the circuit actuation for removal of the fixed pattern noise in the

conventional equipment of the above-mentioned configuration is explained.

[0008] In a level blanking period, if a certain line is chosen by the vertical scanning by the vertical-scanning circuit 104, the signal level at the time of ** before pixel reset of the pixel 101 of the selected line and the signal level at the time of the dark after pixel reset will be sampled by sampling switches 105s and 105n in order, and it will be held by Capacitors 106s and 106n.

[0009] Next, in a level shelf-life, when a certain train is chosen by the horizontal scanning by the horizontal scanning circuit 109 and the level selecting switches 107s and 107n of the selected train turn on in order by it, the signal level at the time of ** held by Capacitors 106s and 106n and the signal level at the time of dark are read to the level signal line 108 one by one. Thereby, on a time-axis, the signal level at the time of ** and the signal level at the time of dark get mixed up per train, are transmitted with the level signal line 108, and are supplied to the CDS circuit 111 through the water Hiraide force circuit 110.

[0010] And in this CDS circuit 111, a correlation duplex sampling with the signal level at the time of ** which gets mixed up on a time-axis, and the signal level at the time of dark is performed, and a noise component is offset by taking that difference. Consequently, the signal with which the fixed pattern noise resulting from property variations, such as the threshold electrical potential difference Vth of a pixel 101, was removed will be acquired.

[0011]

[Problem(s) to be Solved by the Invention] however , in the conventional magnification mold solid state camera mentioned above , when there be a component which ride on a signal in this sample hold circuit since the flow of the signal at the time of ** and dark differed in the sample hold circuit between the perpendicular signal line 103 and the level signal line 108 although it be removable about the fixed pattern noise resulting from the property variation of a pixel 101 , this component remain , even after correlation duplex sample in the CDS circuit 111 .

[0012] Existing as a component which rides from this sample hold circuit has a sampling switches [105s and 105n] distribution noise etc. When this component changes between trains with variations in a circuit property, the component which remains after a correlation duplex sampling will also vary between trains, and this will appear as a vertical-reinforcement-like fixed pattern noise on a screen.

[0013] This invention is made in view of the above-mentioned technical problem, and the place made into the purpose is to offer the solid state camera which can oppress not only the fixed pattern noise resulting from the property variation of a pixel but the fixed

pattern noise of the shape of a vertical reinforcement resulting from the property variation of a circuit, and its drive approach.

[0014]

[Means for Solving the Problem] Two or more pixels by which the solid state camera by this invention was arranged in the shape of a matrix, and the 1st switching means by which the end was connected to the perpendicular signal line to which each outgoing end of these pixels was connected per train, The 1st and the 2nd are recording means which one edge each was connected to the other end of this 1st switching means in common, It has composition equipped with the perpendicular output circuit containing the level selecting switch connected between the other end of the 2nd and 3rd switching means connected, respectively between each other end of these are recording means, and a reference potential point, and the 1st are recording means, and a level signal line for every train.

[0015] In driving the solid state camera of the above-mentioned configuration, the drive approach by this invention is set at a level blanking period. First, make the 1st switching means turn on by the ON state of the 2nd switching means, and the signal at the time of ** is sampled. Then, make the 1st switching means turn off and the signal at the time of ** is held for the 1st accumulation-of-electricity means. Next, the 3rd switching means which is made to turn off the 2nd switching means and is in an OFF state continuously is made to turn on. Next, make the 1st switching means turn on again, sample the signal at the time of dark, and make the 1st switching means turn off again, and hold the signal at the time of dark for the 2nd accumulation-of-electricity means, and, subsequently to a level shelf-life, it is set. Read the electrical potential difference of the output side of the 1st accumulation-of-electricity means to a level signal line, and make a level selecting switch turn on, the 2nd switching means is made to turn on continuously, and a reference potential is read to a level signal line.

[0016] In the solid state camera and its drive approach of the above-mentioned configuration, first, the 1st switching means is made to turn on by the ON state of the 2nd switching means, the signal at the time of ** after pixel reset is sampled, and this is held for the 1st accumulation-of-electricity means by making the 1st switching means turn off at a level blanking period. At this time, the noise component accompanying switching of the 1st switching means rides on the 1st accumulation-of-electricity means. Next, the 2nd switching means is made to turn off. Since the input side of the 1st accumulation-of-electricity means is in floating at this time, the noise component accompanying switching of the 2nd switching means does not ride on the 1st accumulation-of-electricity means.

[0017] Then, make the 3rd switching means turn on, and the 1st switching means is made to turn on again continuously, the signal at the time of the dark which resets a pixel and is obtained is sampled, and this is held for the 2nd accumulation-of-electricity means by making the 1st switching means turn off. Since the 2nd accumulation-of-electricity means is connected to the output side of the 1st switching means at this time, the noise component accompanying switching of the 1st switching means rides on the 2nd accumulation-of-electricity means like the case where the signal at the time of ** is held.

[0018] Consequently, the noise component accompanied by the 1st and the property variation of the circuit used as the cause of the vertical-reinforcement-like fixed pattern noise which rode on the 2nd accumulation-of-electricity means, i.e., switching of the 1st switching means, is canceled by the output side of the 1st accumulation-of-electricity means, and, moreover, a reference potential is added and outputted to the difference of the signal at the time of **, and the signal at the time of dark, i.e., the signal component from which the fixed pattern noise resulting from the property variation of a pixel was removed, at it.

[0019] Subsequently, in a level shelf-life, the signal with which the level selecting switch was made to turn on and the reference potential was added to the electrical potential difference of the output side of the 1st accumulation-of-electricity means, i.e., a signal component, (difference of the signal at the time of ** and the signal at the time of dark) is read to a level signal line. Then, the 2nd switching means is made to turn on and a reference potential is read.

[0020] Thereby, on a time-axis, the signal and reference potential with which the reference potential was added to the signal component get mixed up per train, and are transmitted with a level signal line in a water Hiraide force circuit. And in a latter circuit, the property variation of the circuit between the trains in the perpendicular output circuit which rides common to both signals is canceled by taking the difference of the signal and reference potential with which the reference potential was added to the signal component. Consequently, the signal with which the fixed pattern noise of the shape of a vertical reinforcement resulting from the property variation of not only the fixed pattern noise resulting from the property variation of a pixel but a circuit was removed is acquired.

[0021]

[Embodiment of the Invention] Hereafter, it explains to a detail, referring to a drawing about the gestalt of operation of this invention.

[0022] Drawing 1 is the outline block diagram showing 1 operation gestalt of this

invention. In drawing 1 , many pixels 11 are arranged in the shape of a matrix, the control-input edge of each pixel 11 is connected to each of the perpendicular selection line 12 per line, and each outgoing end is connected to each of the perpendicular signal line 13 per train. From a pixel 11, a signal is outputted to the perpendicular signal line 13 as an electrical potential difference. One edge each of the perpendicular selection line 12 is connected to the outgoing end of each line of the vertical-scanning circuit 14. The vertical-scanning circuit 14 is constituted by the shift register etc., and outputs vertical-scanning pulse phiV (--, phiVm, phiVm+1, --) in order.

[0023] The drain of the sampling switch (the 1st switching means) 15 which consists of a NchMOS transistor is connected to each of the perpendicular signal line 13. Sampling pulse phiVg-SH for reading the signal level at the time of ** before pixel reset and the signal level at the time of the dark which resets a pixel 11 and is obtained (the signal level at the time of the dark after pixel reset being called hereafter) from a pixel 11, respectively is impressed to the gate of this sampling switch 15. One edge each of the load capacitor (1st are recording means) 16 and the dummy capacitor (2nd are recording means) 17 is connected to the source of a sampling switch 15.

[0024] Between the other end of the load capacitor 16, and the reference potential line 18 which gives reference potential V-Ref, the reference switch (the 2nd switching means) 19 which consists of an MOS transistor is connected. Similarly, between the dummy capacitor 17 and the reference potential line 18, the dummy reference switch (the 2nd switching means) 20 which consists of an MOS transistor is connected. In the gate of this reference switch 19, it is reference pulse phiVg-Ref. Dummy reference pulse phiVg-dumy Ref is impressed to the gate of the dummy reference switch 20, respectively.

[0025] The input edge of the perpendicular output circuit 21 is further connected to the other end of the load capacitor 16. The outgoing end of the perpendicular output circuit 21 is connected to the level signal line 22. This perpendicular output circuit 21 consists of level selecting switches 24 which consist of an MOS transistor connected between the source follower circuit 23 which consists of drive MOS transistor Q1 and load MOS transistor Q2 which were connected to the serial between the power source Vdd and the gland, and the source of drive MOS transistor Q1 and the level signal line 22, as shown in drawing 2 . In the source follower circuit 23, predetermined bias voltage Vg-load is impressed to the gate of load MOS transistor Q2.

[0026] The gate of this level selecting switch 24 is connected to the outgoing end of each train of the horizontal scanning circuit 25. The horizontal scanning circuit 25 is constituted by the shift register etc., and outputs horizontal scanning pulse phiH (--,

phiHn, phiHn+1, --) for making the level selecting switch 24 turn on in order. The level signal line 22 is connected to the input edge of the water Hiraide force circuit 26. The outgoing end of the water Hiraide force circuit 26 is connected to the input edge of the CDS (correlation duplex sampling) circuit 27.

[0027] Next, in the magnification mold solid state camera concerning 1 operation gestalt of this invention of the above-mentioned configuration, the drive approach for removing the fixed pattern noise of the shape of a vertical reinforcement resulting from circuit variation is explained with the fixed pattern noise resulting from the property variation of a pixel 11 using the timing chart of drawing 3 .

[0028] First, actuation (t1-t6) until it carries out sample hold of the signal level is explained, referring to the explanatory view of drawing 4 of operation.

[0029] a level blanking period -- setting -- first -- Time t -- the signal level Vsigl at the time of ** before pixel reset is sampled because sampling pulse phiVg-SH will be set to "H" level by 1 and a sampling switch 15 will be in an ON state. At this time, it is reference pulse phiVg-Ref. Since it is in "H" level and the reference switch 19 is in an ON state, the output side potential of the load capacitor 16 is in reference potential V-Ref.

[0030] next, the time t -- in 2, when sampling pulse phiVg-SH will change on "L" level and a sampling switch 15 will be in an OFF state, the signal level Vsigl at the time of ** is held by the load capacitor 16. Under the present circumstances, noise component Valpha accompanying the switching at the time of the cut-off of a sampling switch (SH Tr) 15 rides on the load capacitor 16.

[0031] next, a time -- t3 -- setting -- reference pulse phiVg-Ref It will change on "L" level, this will be answered, and the reference switch 19 will be in an OFF state. Since the input side of the load capacitor 16 is in floating at this time when a sampling switch 15 is in an OFF state, noise component Vbeta accompanying the switching at the time of the cut-off of the reference switch (Ref Tr) 19 does not ride on the load capacitor 16.

[0032] next, a time -- t4 -- dummy reference pulse phiVg-dumy Ref -- " -- after it will be set to H" level and the dummy reference switch 20 will be in an ON state, the signal level Vsigd at the time of the dark after pixel reset is sampled because sampling pulse phiVg-SH will be again set to "H" level and a sampling switch 15 will be in an ON state in t5 at the time.

[0033] next, the time t -- in 6, when sampling pulse phiVg-SH will change on "L" level and a sampling switch 15 will be in an OFF state, the signal level Vsigd at the time of dark is held by the dummy capacitor 17. Under the present circumstances, since the dummy capacitor 17 is connected to the output side of a sampling switch 15, noise

component Valpha accompanying switching of a sampling switch 15 rides on the dummy capacitor 17 like the case where the signal level Vsigl at the time of ** is held.

[0034] Thus, each input side of the load capacitor 16 and the dummy capacitor 17 is connected to the outgoing end of a sampling switch 15. While connecting suitably each output side of these capacitors 16 and 17 to the reference potential line 18 with the reference switches 19 and 20 The signal level by which the correlation duplex sampling was carried out (Vsigd-Vsigl+V-Ref) is drawn by the output side of the load capacitor 16 by connecting with the input edge of the perpendicular output circuit 21, and driving the output side of the load capacitor 16 in the procedure mentioned above.

[0035] Namely, a dummy circuit (the dummy capacitor 17 and dummy reference switch 20) is prepared in the circuit (the load capacitor 16 and reference switch 19) which takes charge of a correlation duplex sampling action, and a symmetrical form. While performing a correlation duplex sampling, by reading the signal level Vsigl at the time of **, and the signal level Vsigd at the time of dark via the same signal path The signal level from which the noise component accompanied by the property variation of the circuit used as the cause of the fixed pattern noise of the shape not only of the fixed pattern noise resulting from the property variation of a pixel 11 but a vertical reinforcement, i.e., switching of a sampling switch 15, was removed is obtained.

[0036] Then, the actuation (t7-t8) which outputs a signal level to the level signal line 22 is explained.

[0037] in a level shelf-life, horizontal scanning pulse phiH (--, phiHn, phiHn+1, --) outputs one by one from the horizontal scanning circuit 25 -- having -- Time t -- when the level selecting switch 24 (see drawing 2) in the perpendicular output circuit 21 of the train which is 7 will be in an ON state, the signal level (Vsigd-Vsigl+V-Ref) of the train is read to the level signal line 22 through the perpendicular output circuit 21.

[0038] next, a time -- t8 -- setting -- reference pulse phiVg-Ref When it will be set to "H" level and the reference switch 19 will be in an ON state, reference potential V-Ref is read to the level signal line 22 through the perpendicular output circuit 21. At this time, dummy reference pulse phiVg-dumy Ref changes on "L" level. However, you may make it dummy reference pulse phiVg-dumy Ref maintain "H" level as it is to drawing 3 , as a broken line shows.

[0039] Thus, if the noise component accompanying switching of the offset variation of the source follower circuit 23 (see drawing 2) or the level selecting switch 24 rides and variation is in these between trains in case it passes through the perpendicular output circuit 21, it will become a vertical-reinforcement-like fixed pattern noise at the signal level (Vsigd-Vsigl+V-Ref) and reference potential V-Ref which were read to the level

signal line 22 one by one.

[0040] However, after the signal level (Vsigd-Vsigl+V-Ref) and reference potential V-Ref which were read to the level signal line 22 one by one getting mixed up per train, transmitting them with the level signal line 22 on a time-axis and passing through the water Hiraide force circuit 26, a correlation duplex sampling is performed in the CDS circuit 27, and the difference is taken. Thereby, the property variation of the circuit between the trains in the perpendicular output circuit 21 used as the cause of a vertical-reinforcement-like fixed pattern noise can be removed.

[0041] The signal with which the fixed pattern noise of the shape of a vertical reinforcement which originates in the property variation of circuits, such as a noise component accompanying switching of not only the fixed pattern noise resulting from the property variation of a pixel 11 but the sampling switch 15, offset variation of the source follower circuit 23 (see drawing 2), and a noise component accompanying switching of the level selecting switch 24, by the above was removed is acquired.

[0042] Moreover, in the conventional magnification mold solid state camera, since the signal level Vsigl at the time of ** before pixel reset and the signal level Vsigd at the time of the dark after pixel reset get mixed up per train and were transmitted on the time-axis, the time amount margin needed to be secured between the signal level Vsigl at the time of **, and the signal level Vsigd at the time of dark, and, as a result, the phase margin of the clock in a horizontal scanning circuit or a latter CDS circuit was not fully able to be secured.

[0043] on the other hand, in the magnification mold solid state camera concerning this invention From it being reference potential V-Ref, following a signal level (Vsigd-Vsigl+V-Ref) per train on a time-axis When reading a signal level (Vsigd-Vsigl+V-Ref) Since reference potential V-Ref can be read succeedingly, namely, it is not necessary to give a time amount margin between a signal level (Vsigd-Vsigl+V-Ref) and reference potential V-Ref, There is also an advantage that the phase margin of the clock in the horizontal scanning circuit 25 or the latter CDS circuit 27 is fully conventionally securable compared with equipment.

[0044] Drawing 5 is the outline block diagram showing other operation gestalten of this invention, among drawing, gives the same sign to drawing 1 and an equivalent part, and is shown.

[0045] At a previous operation gestalt, it is reference pulse phiVg-Ref to the reference switch 19 of each train. With this operation gestalt, it has the composition of giving reference pulse phiVg-Ref (--, phiVg-Ref (n), phiVg-Ref (n+1), --) which is different for every train to the reference switch 19 of each train, to having considered as the

configuration given in common. This reference pulse phiVg-Ref (--, phiVg-Ref (n), phiVg-Ref (n+1), --) is outputted from the horizontal scanning circuit 25.

[0046] The timing chart for explanation of other operation gestalten of operation is shown in drawing 6 . this timing chart -- setting -- a time -- the t1- time t -- it is completely the same as the case of a previous operation gestalt about actuation to 6, i.e., actuation until it carries out sample hold of the signal level, since it overlaps about that explanation, it omits, and the actuation in the case of outputting a signal level to the level signal line 22 is explained below.

[0047] in a level shelf-life, horizontal scanning pulse phiH (--, phiHn, phiHn+1, --) outputs one by one from the horizontal scanning circuit 25 -- having -- Time t -- when the level selecting switch 24 (see drawing 2) in the perpendicular output circuit 21 of n train will be in an ON state by 7, the signal level (Vsigd-Vsigl+V-Ref) of n train is read to the level signal line 22 through the perpendicular output circuit 21.

[0048] next, the time t -- in 8, when reference pulse phiVg-Ref (n) of n train will serve as "H" level and the reference switch 19 of n train will be in an ON state, reference potential V-Ref is read to the level signal line 22 through the perpendicular output circuit 21 of n train. Although "H" level or "L" level is also available for dummy reference pulse phiVg-dumy Ref at this time, in this example, it considers as the useless thing which maintains "H" level as it is so that there may be nothing.

[0049] next, the time t -- in 9, if horizontal scanning pulse phiHn of n train disappears and horizontal scanning pulse phiHn+1 of n+1 train occurs, the level selecting switch 24 of n+1 train will be in an ON state, and the signal level (Vsigd-Vsigl+V-Ref) of n+1 train will be read to the level signal line 22 through the perpendicular output circuit 21. Then, when reference pulse phiVg-Ref (n+1) of n+1 train will serve as "H" level and the reference switch 19 of n+1 train will be in an ON state, reference potential V-Ref is read to the level signal line 22 through the perpendicular output circuit 21 of n+1 train.

[0050] Henceforth, in order, the same actuation covers one line and is performed. Thus, on a time-axis, the signal level (Vsigd-Vsigl+V-Ref) and reference potential V-Ref which were read to the level signal line 22 one by one get mixed up per train, are transmitted with the level signal line 22, and are supplied to the CDS circuit 27 through the water Hiraide force circuit 26. And in the CDS circuit 27, a correlation duplex sampling is performed and the difference is taken.

[0051] The signal with which the fixed pattern noise of the shape of a vertical reinforcement which originates in the property variation of circuits, such as a noise component accompanying switching of not only the fixed pattern noise resulting from the property variation of a pixel 11 but the sampling switch 15, offset variation of the

source follower circuit 23, and a noise component accompanying switching of the level selecting switch 24, as well as the case of a previous operation gestalt by the above was removed is acquired.

[0052] In addition, although considered as the case where a signal is outputted as an electrical potential difference from a pixel 11, with each above-mentioned operation gestalt, the case where a source follower circuit is constructed as this example, using BCMD and CMD as a drive transistor, and resistance of that source follower circuit might be transposed to capacity, and volume load read-out actuation may have been performed.

[0053] In volume load read-out actuation, the load capacitor 16 and the dummy capacitor 17 are used as a load at the time of read-out at the time of read-out at the time of **, and dark, respectively. However, addition of means (transistor etc.) to reset the perpendicular signal line 13 to fixed potential just before reading the signal at the time of ** and dark to the circuit of this invention in volume load actuation is needed.

[0054]

[Effect of the Invention] As explained above, according to this invention, in the circuit which reads the signal level at the time of **, and the signal level at the time of dark from each pixel to a level signal line, it becomes possible by having made the same the read-out path of both signal levels to oppress not only the fixed pattern noise resulting from the property variation of a pixel but the fixed pattern noise of the shape of a vertical reinforcement resulting from the property variation of a circuit.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the outline block diagram showing 1 operation gestalt of this invention.

[Drawing 2] It is the circuit diagram showing an example of the configuration of a perpendicular output circuit.

[Drawing 3] It is a timing chart for explanation of 1 operation gestalt of this invention of operation.

[Drawing 4] It is the explanatory view of 1 operation gestalt of this invention of operation.

[Drawing 5] It is the outline block diagram showing other operation gestalten of this invention.

[Drawing 6] It is a timing chart for explanation of other operation gestalten of this invention of operation.

[Drawing 7] It is the outline block diagram showing the conventional example.

[Description of Notations]

11 Pixel 13 Perpendicular Signal Line 14 Vertical-Scanning Circuit

15 Sampling Switch 16 Load Capacitor

17 Dummy Capacitor 18 Reference Potential Line

19 Reference Switch 20 Dummy Reference Switch

21 Perpendicular Output Circuit 22 Level Signal Line 23 Source Follower Circuit

24 Level Selecting Switch 25 Horizontal Scanning Circuit 26 Water Hiraide Force Circuit

27 CDS Circuit